UNIVAC

DIVISION OF SPERRY RAND CORPORATION

SPECIFICATION APPROVAL SHEET CONTINUATION

SHEET 1.3	REVISION E

SPECIFICATION SYMBOL
SB-10163

SHEET INDEX

SHEET	686	687	688	689	690	691	692	693	694	695	696	697	698	699	700	701	702	703	704	705	706	707
REV.	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

SHEET	708	709	710	711	712	713	714	715	716	717	718	719	720	721	722	723	724	725	726	727	728	729
REV.	—	—	—	—	—	—	—	—	—	—	—	—	—	C	C	—	—	C	—	—	—	—

SHEET	730	731	732	733	734	735	736	737	738	739	740	741	742	743	744	745	746	747	748	749	750	751
REV	—	—	C	—	—	—	—	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C

SHEET	752	753	754	755	756	757	758	759	760	761	762	763	764	765	766	767	768	769	770	771	772	773
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	—	C	—	C	B	B

SHEET	774	775	776	777	778	779	780	781	782	783	784	785	786	787	788	789	790	791	792	793	794	795
REV	—	C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

SHEET	796	797	798	799	800	801	802	803	804	805	806	807	808	809	810	811	812	813	814	815	816	817
REV	—	—	—	—	—	—	C	C	C	—	—	—	—	—	—	C	C	C	—	—	—	—

SHEET	818	819	820	821	822	823	824	825	826	827	828	829	830	831	832	833	834	835	836	837	837	839
REV	—	—	—	—	—	—	—	—	—	—	—	—	—	C	C	—	—	—	C	C	C	C

SHEET	840	841	842	843	844	845	846	847	848	849	850	851	852	853	854	855	856	857	858	859	860	861
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C

SHEET	862	863	864	865	866	867	868	869	870	~~871~~	~~872~~	~~873~~	~~874~~	~~875~~	~~876~~	~~877~~	~~878~~	~~879~~	~~880~~	~~881~~	~~882~~	~~883~~
REV	C	C	C	C	C	C	C	C	E				~~B~~	~~B~~	~~B~~	~~B~~	~~B~~	~~B~~	~~B~~	~~B~~	~~B~~	~~B~~

SHEET	~~884~~	~~885~~	~~542.1~~	~~542.2~~	~~542.3~~	~~542.4~~	~~542.5~~	728.1	728.2	728.3	728.4	728.5
REV	~~B~~	~~B~~	~~B~~	~~B~~	~~B~~	~~B~~	~~B~~	C	C	C	C	C

SHEET	728.6	728.7	728.8	728.9	765.1	765.2	765.3	765.4	765.5	~~765.6~~	~~765.7~~
REV	C	C	C	C	C	C	C	C	D	~~C~~	~~C~~

SHEET	821.1	821.2	821.3	821.4	821.5	821.6	821.7
REV	C	C	C	C	C	C	C

SHEET																						
REV																						

SHEET																						
REV																						

COMPUTER, DIGITAL DATA - UNIVAC 1219B
PART NO. 7049747
ACCEPTANCE PROCEDURES FOR

1. INTRODUCTION

1.1 Purpose. - This specification establishes the inspection required to prove that the UNIVAC 1219B Computer (hereinafter referred to as the Computer) meets the requirements of SB-10157. The inspection specified herein forms a basis for acceptance or rejection by the procuring activity.

1.2 Applicable documents. - The following documents form a part of this specification to the extent specified herein. Unless otherwise indicated, the latest issue in effect shall apply.

SPECIFICATIONS

Sperry Univac

DS 4772	Interface Characteristics, UNIVAC Defense Computer Equipment
SB 10163-400	Test Summary Form Computer, UNIVAC Type 1219

DRAWINGS

Sperry Univac

7049747	Computer, Digital Data, UNIVAC 1219B

PUBLICATIONS

Sperry Univac

PX 3288	Programmers Reference Manual for UNIVAC 1219B Computer

1.3 Applicability of inspection. - The inspections specified herein permit acceptance or rejection, by the procuring activity of all configurations of the Computer. As such, certain sections of the inspections apply only to a specific configuration of the Computer and these sections shall be omitted whenever the Computer being inspected is not of that configuration. See PX 3316 for detailed reference designations.

Example: The basic Computer configuration does not contain an A8,A9,A10, or A13 module; therefore any inspection specified herein which refers to A8,A9,A10 or A13 will not be applicable if the configuration of the Computer does not include these modules.

1.4 Inspection conditions. - Unless otherwise specified in the applicable equipment specification, the inspection shall be performed at room ambient temperature, humidity, and atmospheric pressure.

1.5 Inspection evaluation. - Any error (see 5.1) that occurs shall be evaluated in accordance with Section 4 prior to resuming the inspection.

1.6 Inspection sequence. - The inspection specified herein shall be performed in the following sequence:

a. Nonprogrammed inspection (Section 2)

b. Programmed inspection (Section 3).

1.7 Test equipment. - The following test equipment, or equivalent, shall be used while performing the inspection specified herein.

Item	Description
1	Oscilloscope, Tektronix Model 585
2	Preamplifier, Tektronix Model 82
3	DC Voltmeter, 0.5 percent accuracy, Weston Model 931
4	Hot Air Gun, 150 watts maximum power
5	AC Voltmeter, 0.5 percent accuracy, 25 to 400 Hertz, Weston Model 433
6	Timer, Beckman/Berkely, Model 8370
7	Input/Output Console, UNIVAC 1232
8	Cables, Interconnecting in accordance with DS 4772
9	Computer Remote Control in accordance with 7029664
10	Bootstrap Assembly, 7024774-02
11	Variac, three phase, TX 31563
12	Shielded Wire

Item	Description
13.	Program Tape, Input/Output Mode Test (SB-10163-1, revision 1)
14.	Program Tape, Integrated Command-Arithmetic Test, (SB-10163-2, -4, and -5, revision 1)
15.	Program Tape, Integrated Memory Test, (SB-10163-3, -6, and -7, revision 1)
16.	Program Tape, Input/Output Signal Test, (SB-10163-8, revision 1)

1.8 Inspection record. - Record the inspection results in the Test Summary Form SB-10163-400.

2. NONPROGRAMED INSPECTION

2.1 Surface examination. - The Computer shall be examined for conformance to the materials, parts, processes, finish, size, weight, and workmanship requirements specified on Drawing 7049747 and the drawings and specifications referenced thereon.

2.2 Input power blower rotation, and power controls. - Unless otherwise specified, no program shall be in process in the Computer and the initial switch positions shall be as specified in table I.

Table I. Initial Switch Positions

Switch(es)	Position
POWER	OFF
DISC ALARM/RESET ALARM	neutral
BATTLE SHORT	OFF
INDICATE-OFF-INDICATE/SET	INDICATE/SET
CHANNEL INTER-COMPUTER/CHANNEL NORMAL	CHANNEL NORMAL
CHANNEL FUNCTION	SINGLE
I/O CLEAR-MASTER CLEAR	neutral
SEQ STEP/STOP	neutral
RESTART SPEED CONTROL	approximate center
RESTART/START STEP	neutral
FUNCTION REPEAT	released (see 5.1)
PHASE REPEAT	released
AUTO RECOVERY	released
DISC ADV P	released
PROGRAM STOPS	released
PROGRAM SKIPS	released
EXT SYNC DISC	selected
RTC DISC	selected
CLOCK (behind A2 panel)	NORMAL
BOOTSTRAP MODE	NDRO

The input power shall be applied and the power controls shall be tested as follows. The number and locations of blowers shall be subject to the optional configurations.

a. Input power - Using the ac voltmeter (Item 5) and the variac (Item 11), apply 115 volts (average of three line-to-line voltages) ±5 percent, 3 phase, 400 cycles per second ±5 percent to the following pins (measure at the output of the variac):

   A14 J1-A (Phase A)
   A14 J1-B (Phase B)
   A14 J1-C (Phase C)
   A14 J1-D (Ground)

b. Momentarily operate the POWER switch to ON (turn on the power).

c. Observe (see 5.1) that the POWER and LOCAL CONTROL indicators light (see 5.1).

d. Using the variac and the ac voltmeter at the variac output, measure the three line-to-line voltages and adjust, if necessary, to 115 volts ± 1%.

e. Master Clear (see 5.1).

f. Momentarily operate the POWER switch to OFF (turn off the power).

g. Observe that the POWER and LOCAL CONTROL indicators extinguish.

h. Open the A5 and A10 air intakes and remove the A5 and A10 air filters.

i. Turn on the power (see 5.1).

j. Observe that the blowers mounted in A5 and A10 rotate so that the bottom of the rotor moves toward the front of the Computer.

k. Turn off the power (see 5.1).

l. Replace the A5 and A10 air filters and close A5 and A10.

m. Turn on the power and observe that the A6 blower is rotating to cause air flow as shown in figure 1.

CAUTION: To prevent possible tipping of the Computer, if not securely fastened, do not have more than one chassis extended.

2.3 Power supply interlock test. - Perform the following steps:

a. Loosen the fasteners and slide the power-supply (PS1) drawer forward.

b. Observe that the POWER indicator extinguishes (this indicates that power has been removed).

c. Momentarily operate the POWER switch to ON.

d. Observe that the POWER indicator does not light.

e. Operate the interlock switch S1 forward (latches).

f. Momentarily operate the POWER switch to ON.

g. Observe that the POWER indicator lights.

h. Momentarily operate the POWER switch to OFF.

i. Return the interlock switch to the neutral position.

j. Operate the BATTLE SHORT switch to ON.

k. Momentarily operate the POWER switch to ON.

l. Observe that the POWER indicator lights.

m. Operate the BATTLE SHORT switch to OFF.

n. Observe that the POWER indicator extinguishes.

o. Return the power-supply drawer to its original position and fasten.

CAUTION: Do not leave the power-supply drawer in the extended position with power applied for more than 15 minutes.

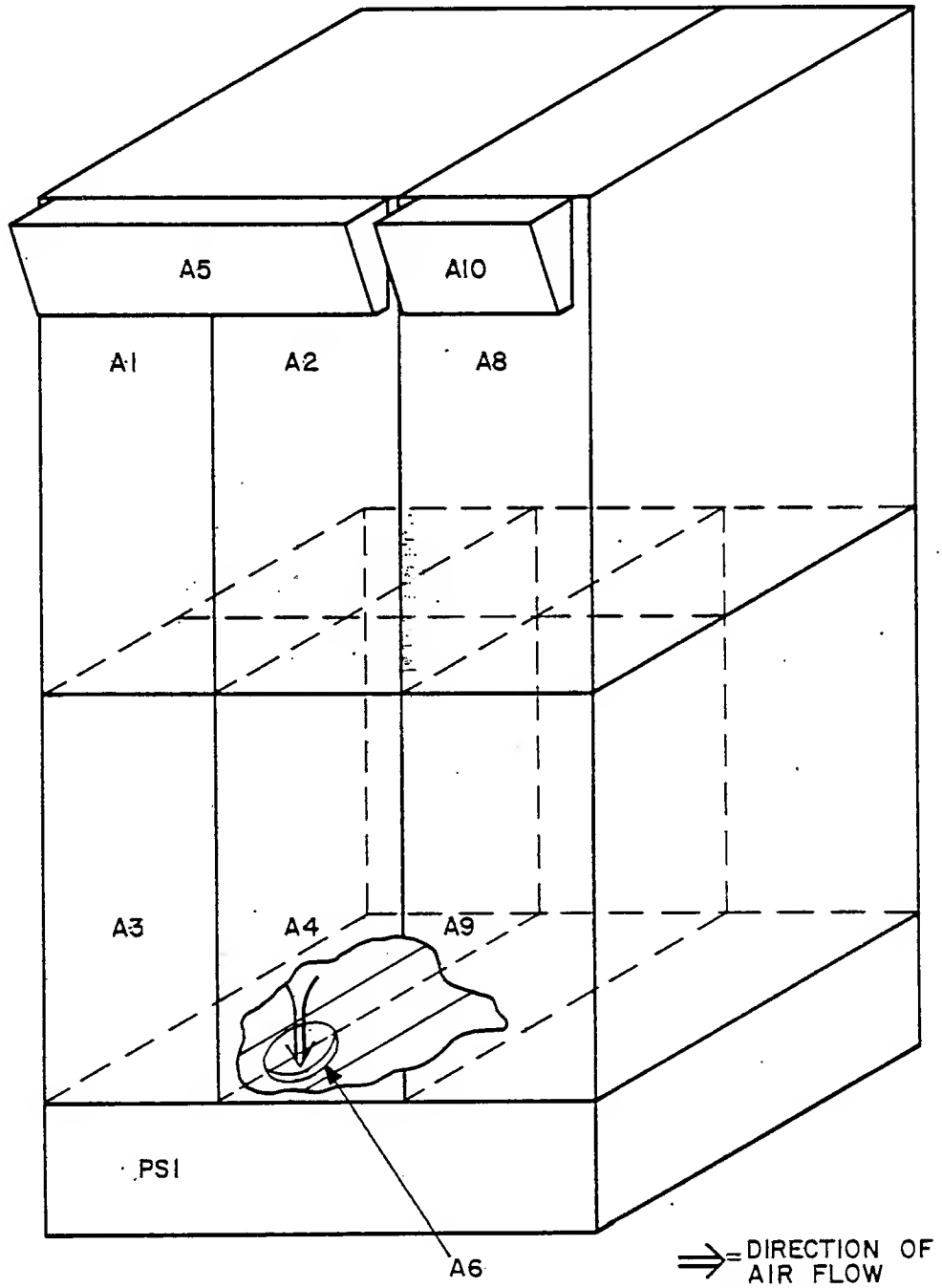

Figure 1. 1219B Blower Location and Air Flow Direction

2.4 Overtemperature abnormal condition test. - Perform the following steps:

a. Place the hot air gun (Item 4) near thermostat S2 (115°F thermostat). Access to the thermostats is obtained by pulling out the A3 chassis.

b. Momentarily operate the POWER switch to ON.

c. Observe that after a period of time the ABNORMAL CONDITION and the TEMP indicators light and that the alarm sounds.

d. Operate the BATTLE SHORT switch to ON.

e. Observe that the ABNORMAL CONDITION and TEMP indicators remain lit and that the alarm stops sounding.

f. Operate the BATTLE SHORT switch to OFF.

g. Observe that the alarm sounds.

h. Select DISC ALARM.

i. Observe that the alarm still sounds.

j. Select RESET ALARM.

k. Observe that the ABNORMAL CONDITION and TEMP indicators remain lit and that the alarm stops sounding.

l. Remove the hot air gun from near S2.

m. Observe, after the thermostat has had time to cool, that the TEMP and ABNORMAL CONDITION indicators extinguish.

n. Place the hot air gun near thermostat S3 (140°F thermostat).

o. Observe that after a period of time the POWER indicator extinguishes.

p. Momentarily operate the POWER switch to ON.

q. Observe that the POWER indicator does not light.

r. Operate the BATTLE SHORT switch to ON.

s. Momentarily operate the POWER switch to ON.

t. Observe that the POWER indicator lights.

u. Operate the BATTLE SHORT switch to OFF.

v. Observe that the POWER indicator extinguishes.

w. Remove the hot air gun from near S3.

x. After S3 has cooled, momentarily operate the POWER switch to ON.

y. Observe that the POWER indicator lights.

z. Momentarily operate the POWER switch to OFF.

aa. Return A3 to the operating position and fasten.

ab. Place the hot air gun near thermostat S4 (115° F thermostat). Access to the thermostat is obtained by opening the A9 blank panel.

ac. Repeat steps b through m for S4.

ad. Repeat steps n through z for S5.

ae. Return the A9 blank panel to the operating position and fasten.

2.5 Voltage fault abnormal condition test. -

a. Turn on the power.

b. Set (see 5.1) RUN MODE.

c. Using the variac, slowly lower the 115 vac three phase input voltage. (Monitor the input voltage at the output of the variac, using the ac voltmeter)

d. Observe that the ABNORMAL CONDITION and VOLTAGE FAULT indicators light and that the alarm sounds before the input voltage reaches 103 vac, but not before the input voltage reaches 105 vac.

e. Select DISC ALARM.

f. Observe that the alarm still sounds.

g. Momentarily select RESET ALARM.

h. Observe that the alarm still sounds when the RESET ALARM switch is released.

i. Observe that the Computer is Master Cleared.

j. Momentarily operate the RESTART/START STEP switch to START STEP several times.

k. Observe that the Computer remains Master Cleared.

l. Operate the BATTLE SHORT switch to ON.

m. Observe that the ABNORMAL CONDITION and VOLTAGE FAULT indicators are lit and that the alarm stops sounding.

n. Master Clear.

o. Set LOAD MODE.

p. Start the Computer (see 5.1).

q. Observe that the Computer runs and the P register displays any number from 500 to 537.

r. Stop the Computer (see 5.1).

s. Using the ac voltmeter and the variac, adjust the 115 vac three phase input voltage to 115 vac.

t. Operate the BATTLE SHORT switch to OFF.

u. Observe that the alarm sounds.

v. Select RESET ALARM.

w. Observe that the ABNORMAL CONDITION and VOLTAGE FAULT indicators extinguish and the alarm stops sounding.

x. Set the VOLTAGE FAULT indicator-switch.

y. Master Clear.

z. Observe that the VOLTAGE FAULT indicator extinguishes.

2.5.1 Inhibit lockout test.-

a. Extend the A3 chassis.

b. Operate the BATTLE SHORT switch to ON.

c. Connect the oscilloscope (Item 1) and the preamplifier (Item 2) to A3A2J11C-TP1. Ground the oscilloscope at A3A2W2.

d. Using the variac (Item 11) and the ac voltmeter (Item 5) lower the 115 vac three phase input voltage to a point below 100 vac (approximately 95 vac).

e. Slowly increase the input voltage and observe that the output switches from +3 vdc to 0 vdc before the voltage reaches 102 vac, but not before the input voltage reaches 100 vac.

f. Adjust the input voltage to 115 vac.

g. If the computer configuration includes the A3A1 chassis, repeat steps c through f except in step c connect the oscilloscope to A3A1J11C-TP1 and ground at A3A1W2; otherwise proceed to the next step.

h. Remove the oscilloscope connections, return chassis A3 to the normal position and fasten.

i. Operate the BATTLE SHORT switch to OFF.

2.6 Power supplies. - Using the ac voltmeter and the variac, determine that the input voltages are as specified in 2.2. Master Clear the Computer, set PHASE STEP MODE, and using the oscilloscope (Item 1), the preamplifier (Item 2), and the dc voltmeter (Item 3), measure each of the power supply voltages specified in table II. Use a direct probe with the oscilloscope and preamplifier when measuring the ripple voltages.

2.7 Running time meter. - Perform the following steps:

a. Momentarily operate the POWER switch to ON.

b. Observe that the RUNNING TIME meter indicates the power on time to the nearest tenth of an hour, and that the indicator wheel is turning.

Table II. Power Supply Voltages

Supply Voltage	Voltage Range (volts)	Maximum Ripple (volts)**	Test Point	Ground
-15*	-13.5 to -16.5	0.2	A2A1 TB1-E33	A2A1 TB1-G33
-4.5	-4.05 to -4.95	0.2	A2A1 TB1-F33	
+15*	+13.5 to +16.5	0.2	A2A1 TB1-D33	
+3	+2.9 to +3.1	0.1	A3A1J7C-TP9 A3A2J7C-TP9	A3A2W2
+6	+5.7 to +6.3	0.1	A3A1J7C-TP1 A3A2J7C-TP1	A3A2W2
+Reg	Preset for optimum Control Memory operation	0.1	A4A2TB2-C33	A4A2TB2-G33
-Reg		0.1	A4A2TB2-B33	

* The difference between the absolute values of these voltages shall not be greater than 6 percent of the smaller voltage (absolute value).

** When the Computer is Master Cleared and Phase Step mode is selected.

2.8 Indicate-Off-Indicate/Set test. - Perform the following operations:

a. Operate the INDICATE-OFF-INDICATE/SET switch to INDICATE/SET.

b. Set OP STEP MODE.

c. Master Clear.

d. Set several indicator-switches on each of A1, A2, A4, and A8.

e. Operate the INDICATE-OFF-INDICATE/SET switch to OFF.

f. Observe that all indicators set in step d on A1, A2, A4, and A8 extinguish.

Clock	Test Points
1	A2A1 TB1-G32
2	A2A1 TB1-F32
3	A2A1 TB1-E32
4	A2A1 TB1-D32

g. Operate several indicator-switches on each of A1, A2, A4, and A8.

h. Observe that the indicators operated in step g do not light.

i. Operate the INDICATE-OFF-INDICATE/SET switch to INDICATE.

j. Observe that the indicators set in step d light.

k. Operate several indicator-switches on each of A1, A2, A4, and A8.

l. Observe that the indicators operated in step k do not light.

m. Operate the INDICATE-OFF-INDICATE/SET switch to INDICATE/SET.

2.9 Indicators and Master Clear test. -

a. Master Clear.

b. Set PHASE STEP MODE.

c. Operate the BATTLE SHORT switch to ON.

d. Set all indicator-switches, at the discretion of the cognizant Purchaser's Representative except RUN MODE, OP STEP MODE, LOAD MODE, TEMP and VOLTAGE FAULT.

e. Set OP STEP MODE (some indicators set in step d may clear at this time).

f. Master Clear.

g. Operate the BATTLE SHORT switch to OFF.

h. Observe that all indicators set in step d clear (see 5.1) except T11 and the PHASE indicators (if set), and that the OP STEP MODE indicator remains set. Indicators in the B register and the DUAL indicator may or may not clear.

2.10 Registers and designators with manual clear. - Perform the following steps:

a. Set OP STEP MODE.

b. Master Clear.

c. Set each indicator-switch of the registers and designators specified in table III.

d. Operate the clear switch (the clear switch is the white pushbutton switch located adjacent to the register or designator) for each of the registers or designators.

e. Observe that only the indicators specified as Manual Clear in table III clear when the corresponding clear switch is operated

2.11 Registers and designators with I/O clear. - Perform the following steps:

a. Set OP STEP MODE.

b. Master Clear.

c. Set each indicator-switch of the registers and designators specified in table III.

d. Momentarily operate the I/O CLEAR-MASTER CLEAR switch to I/O CLEAR.

e. Observe that only the indicators specified as I/O Clear in table III clear.

Table III. Clear Functions

Register or Designators		Clear Method		
		Manual	Master	I/O
C_O, C_E, EF MODE	Set on both A1 and A8		X	X
EI MON			X	
EF MON, OE MON, ID MON, EF ACT,			X	X
OD ACT, ID ACT, EF/OD ACT,			X	X
ID ACT			X	X
A_U, A_L, ICR, SR		X	X	
SEQ DES, FUNCTION CODE and FII		X	X	
P		X	X	
PHASE (all set when one is set)		X		
S1, Z1		X	X	
I/O TRANSLATOR (DUAL is cleared only in RUN MODE)		X	X	X
B		X		

2.12 Master clock test. - Perform the master clock test as follows:

a. Master Clear.

b. Set OP STEP MODE.

c. Using the oscilloscope and preamplifier, observe the master clock phase pulses at the test points specified in table IV, for both the NORMAL and the NARROW position of the CLOCK switches (ODD switch for phases 1 and 3 and EVEN switch for phases 2 and 4). The CLOCK switches are located inside the A2 panel.

d. Observe:

(1) that each clock phase pulse is from 80 to 120 nanoseconds wide at the minus 2 volt amplitude point with the CLOCK switch in the NORMAL position, and that there is no overlap between phases.

(2) that the pulse width of the clock phase pulse decreases when the corresponding CLOCK switch is in the NARROW position.

(3) that the MARGIN indicator lights when any switch is in the NARROW position.

e. Operate the CLOCK switches to NORMAL.

Table IV. Clock Phase Test Points

Clock Phase	Test Points	
1	A2A1 TB1-G32	1st level drivers
2	A2A1 TB1-F32	
3	A2A1 TB1-E32	
4	A2A1 TB1-D32	

2.13 Phase repeat test. - Perform the following steps:

a. Master Clear.

b. Set PHASE STEP MODE.

c. Manually clear the PHASE indicators.

d. Select PHASE REPEAT.

e. Set PHASE 1.

f. Using the oscilloscope and preamplifier, observe at the corresponding test point specified in table IV, that the phase set in step e is repeated at the normal master clock rate and that the other phases have no signal.

g. Repeat steps c, e, and f for PHASE 2, PHASE 3, and PHASE 4.

h. Manually clear the PHASE indicators.

i. Release (see 5.1) PHASE REPEAT.

2.14 Main memory cycle time. - The main memory cycle time shall be tested as follows:

a. Set RUN MODE.

b. Master Clear.

c. Select FUNCTION REPEAT.

d. Set the FUNCTION CODE register equal to 10. (Unless otherwise specified all register settings and indications are in octal code).

e. Start the Computer.

f. Observe that the PROGRAM RUN indicator lights and, using the timer (item 6), observe that the initiate-main-memory-timing flip-flop signal at A4A1 TB2 G25, has a one second count of between 490,000 and 510,000.*

g. Stop the Computer.

h. Release FUNCTION REPEAT.

2.15 Program stops and skips test. - The program stops and skips shall be tested as follows:

a. Master Clear.

b. Manually load (see 5.1) the program specified in table V.

*This test verifies the master clock rate of 500 ± 10 nanoseconds and the control memory cycle time of 500 ± 10 nanoseconds.

Table V. Manual Program

Address	Instruction	Description
00020	505001	Skip on SKIP 0
00021	505601	Stop on STOP 0
00022	505002	Skip on SKIP 1
00023	505602	Stop on STOP 1
00024	505004	Skip on SKIP 2
00025	505604	Stop on STOP 2
00026	505010	Skip on SKIP 3
00027	505610	Stop on STOP 3
00030	505020	Skip on SKIP 4
00031	505620	Stop on STOP 4
00032	505640	Stop on STOP 5
00033	340020	Jump → 00020

c. Set RUN MODE

d. Set the P register equal to 00020

e. Select all PROGRAM STOPS

f. Momentarily operate the RESTART/START STEP switch to START STEP.

g. Observe that the PROGRAM STOP 0 indicator lights.

h. Operate the RESTART/START STEP switch to START STEP several times.

i. Observe that the Computer operates with the PROGRAM STOP 0, 1, 2, 3, 4, and 5 indicators lighting and extinguishing in sequence, at a rate governed by the START STEP switch operation.

j. Operate the RESTART/START STEP switch to RESTART.

k. Observe that the Computer operates with the PROGRAM STOP 0, 1, 2, 3, 4, and 5 indicators lighting and extinguishing in sequence, at a rate governed by the RESTART SPEED CONTROL (clockwise = faster, counter-clockwise = slower).

l. Select the PROGRAM SKIP switches.

m. Observe that, as a PROGRAM SKIP switch is selected its corresponding PROGRAM STOP indicator no longer lights. (The 5 STOP indicator remains lit.)

n. Release RESTART.

o. Release all PROGRAM STOPS and PROGRAM SKIPS.

2.16. OP step mode, sequence step mode, and function repeat test. - Perform the following steps:

a. Master Clear.

b. Select FUNCTION REPEAT.

c. Set the FUNCTION CODE register equal to 10.

d. Set OP STEP MODE.

e. Momentarily operate the RESTART/START STEP switch to START STEP several times.

f. Observe that the SEQ DES RI indicator is lit and that the FUNCTION CODE register display is not altered by operating the RESTART/START STEP switch.

g. Operate the SEQ STEP/STOP switch to SEQ STEP.

h. Momentarily operate the RESTART/START STEP switch to START STEP several times.

i. Observe that SEQ DES RI and I alternately light and extinguish each time the RESTART/START STEP switch is operated.

j. Release FUNCTION REPEAT.

k. Release SEQ STEP.

2.17 Phase step mode test. - Perform the following steps:

a. Manually load the program specified in table V if it is not already in memory.

b. Master Clear.

c. Set the P register equal to 00020.

d. Set PHASE STEP MODE and clear the PHASE indicators.

e. Select one of the four phases by setting the corresponding PHASE indicator-switch (1, 2, 3, or 4).

f. Momentarily operate the RESTART/START STEP switch to START STEP several times.

g. Observe that for each operation to START STEP the PHASE indicators indicate a one phase advance.

h. Operate the RESTART/START STEP switch to RESTART.

i. Observe that the phase indicators light in sequence at a rate governed by the RESTART SPEED CONTROL.

j. Release RESTART.

k. Set OP STEP MODE.

l. Master Clear.

2.18 DISC ADV P switch test. - The DISC ADV P switch shall be tested as follows:

a. Manually load the program specified in table V if it is not already in memory.

b. Set RUN MODE.

c. Master Clear.

d. Select DISC ADV P.

e. Set the P register equal to 00020.

f Momentarily operate the RESTART/START STEP switch to START STEP.

g. Observe that 50 is displayed in the FUNCTION CODE register. the FORMAT II indicator is lit, and 00020 is displayed in the P register.

h. Release DISC ADV P.

i. Observe that the Computer 5-Steps (see 5.1).

2.19 Program fault test. - The PROGRAM FAULT indicator shall be tested as follows:

a. Set CP STEP MODE.

b. Master Clear (this sets the FUNCTION CODE register equal to 00).

c. Select FUNCTION REPEAT.

d. Start the Computer.

e. Observe that the PROGRAM FAULT indicator lights and the alarm sounds.

f. Select DISC ALARM.

g. Observe that the alarm stops sounding and that the PROGRAM FAULT indicator remains lighted.

h. Release DISC ALARM.

i. Observe that the alarm sounds.

j. Momentarily select RESET ALARM.

k. Observe that the alarm momentarily stops sounding and the PROGRAM FAULT indicator momentarily extinguishes.

l. Master Clear.

m. Observe that the alarm stops sounding and the PROGRAM FAULT indicator extinguishes.

n. Set the FUNCTION CODE register equal to 01.

o. Repeat steps d through m.

p. Set the FUNCTION CODE register equal to 77 and repeat steps d through m.

q. Release FUNCTION REPEAT.

2.20 Auto recovery switch and load mode test. - The auto recovery and load mode test shall be performed as follows:

a. If the Computer does not have the automatic recovery bootstrap program for the input/output console (Item 7), channel 0, remove the bootstrap assembly and replace with bootstrap assembly 7024774-02 (Item 10). The bootstrap assembly is located in A4A2, jacks B20 through B23.

b. Master Clear.

c. If bootstrap assembly is used, operate BOOTSTRAP MODE switch to NDRO. If the bootstrap program located at memory locations 500_8 through 537_8 in main memory is used, operate the BOOTSTRAP MODE switch to MAIN MEMORY.

d. Manually load 000000 at address 01000 and 505640 at address 00000.

e. Set RUN MODE.

f. Set the P register equal to 01000.

g. Start the Computer.

h. Observe that the PROGRAM FAULT indicator lights, the alarm sounds, the S1 register equals 00000, and the PROGRAM STOP 5 indicator is lit.

i. Select DISC ALARM.

j. Observe that the alarm stops sounding.

k. Master Clear.

l. Select AUTO RECOVERY.

m. Set the P register equal to 01000.

n. Set OP STEP MODE.

o. Start the Computer.

p. Observe that the PROGRAM FAULT and LOAD MODE indicators light.

q. Start the Computer.

r. Observe that the PROGRAM FAULT, PROGRAM RUN, and RUN MODE indicators light.

s. Stop the Computer.

t. Observe that the P register displays any number from 500 to 537.

u. Master Clear.

v. Release AUTO RECOVERY.

w. Release DISC ALARM.

2.21 Bootstrap modes test. - The bootstrap modes test shall be performed as follows:

a. Operate BOOTSTRAP MODE switch to MAIN MEMORY.

b. Manually load 525252_8 into memory locations 500_8 through 537_8.

c. Observe that the data in step b can be loaded.

d. Operate the BOOTSTRAP MODE switch to NDRO.

e. Attempt to manually load 111111_8 into memory locations 500_8 through 537_8.

f. Observe that the contents of these locations still contain the bootstrap program specified in 2.20.

g. Operate the BOOTSTRAP MODE switch to MAIN MEMORY.

h. Observe that the contents of memory locations 500_8 through 537_8 still contain 525252_8.

i. Operate the BOOTSTRAP MODE switch to NDRO.

s. Momentarily operate the START/MASTER CLEAR switch to START.

t. Observe that the PROGRAM FAULT and RUN indicators light, the alarm sounds, and that the P register on the Computer displays any number from 500 to 537.

u. Momentarily operate the LOAD/STOP switch to STOP.

v. Observe that the RUN indicator extinguishes.

w. Momentarily operate the START/MASTER CLEAR switch to MASTER CLEAR.

x. Observe that the PROGRAM FAULT indicator extinguishes and that the alarm stops sounding.

y. Operate the AUTO RECOVERY and the REMOTE switch to OFF.

z. Disconnect the Computer Remote Control from the Computer.

2.2[illegible] External synchronizing interrupt test. - The external synchronizing interrupt test shall be performed as follows:

a. Master Clear.

b. Manually load the program specified in table VI.

c. Using a shielded wire (Item 12), connect J18-C (signal) to A2A1 TB2-A33 for a slow interface Computer or to A2A1 TB2-D10 for a fast interface Computer and connect J18-A (ground return) to chassis ground.

d. Select EXT SYNC DISC.

e. Set RUN MODE.

f. Master Clear.

g. Set the P register equal to 00021.

h. Start the Computer.

i. Observe that all zeros are displayed in the A_L register.

j. Release EXT SYNC DISC.

k. Vary the setting of the RESTART SPEED CONTROL.

l. Observe that the contents of the A_L register increase at a rate governed by the RESTART SPEED CONTROL.

m. Stop the Computer.

n. Select EXT SYNC DISC.

o. Disconnect the shielded wire connected in step c.

p. Master Clear.

Table VI. Synchronizing Interrupt Program

Address	Instruction	Description
000016	540017	Indirect Jump and Enable Interrupt
000017	000020	
000020	710001	Add one to A
000021	502400	Wait for interrupt

2.24 Real time clock. - Using the timer, measure the real time clock frequency over a 10 second period. Measure the real time clock frequency at A4A1 TB2-A11. Observe that the 10 second count is 10240 ± 2 count (the real time clock must be enabled).

3. PROGRAMED INSPECTION

3.1 Description and test setup. - The programed inspection exercises the Computer and includes testing of input/output operations, command functions, arithmetic operations, and memory. The Appendix to this specification contains descriptions of programs, including flow charts, data pages, and program listings. Unless otherwise specified, all controls, indicators, and switches are located on the Computer. The referenced programs may be loaded into the Computer memory by utilizing programs and loading procedures specified in PX 3288. Connect the Computer as specified in figure 2 to perform the programed inspection. If necessary, operate switches to initial positions as specified in table I.

NOTE: Printed wiring assembly 7104010 must be inserted in position A4A1J4G for 1219 normal mode operation.

3.2 Input/output signals test. - This test will cycle selected input/output programs on selected channels to permit measuring the input/output signals. The input/output signals test shall be performed as follows:

a. Load the Input/Output Signals test program (SB-10163-8) specified in the Appendix. The program skips and stops of this program are as specified in table VII and the Appendix.

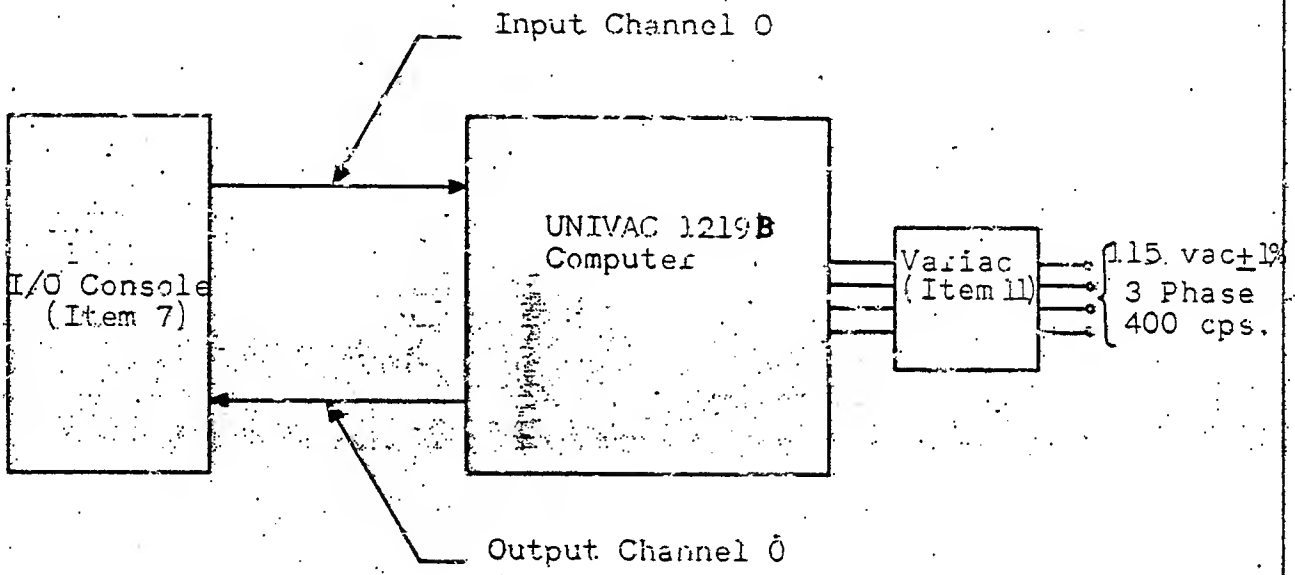

Figure 2. Programed Inspection Test Configuration

Table VII. Input/Output Signals Test Skips and Stops

Switch (es) Selected	Program Action
PROGRAM SKIP 0	External function mode subtest
PROGRAM SKIP 4	5-Stop at end of selected subtest
STOP 2	Stop at end of subtest
STOP 5	Program stop to manually change mode or channel selection

b. Select RTC DISC, EXT SYNC DISC.

c. Set RUN MODE.

d. Master Clear the Computer.

e. Set the P register equal to 01000.

f. Start the Computer.

g. Observe that the Computer 5-Stops.

h, Using interconnecting cables (Item 8), connect all channel pair combinations, except for channel 0 which is connected to the I/O console, specified in table VIIa. (Only one pair of channels per chassis shall be tested.)

i. Set the bits in A_U and A_L as specified in table VIIa in accordance with the channel pair combination being input/output signal tested.

j. Select the normal input/output mode as specified in table VIII with no program skip switches selected.

k. Start the Computer.

l. Observe that the Computer runs.

Table VIIa. Input/Output Channel Connections for Test Configuration

Section	Channel Pair Combinations		Chassis Number	Channel combinations to be input/output signal tested	Bits to be set in A_U	Bits to be set in A_L
Lower	Output	Input				
Eight	0	2	A1A2	No	none	none
	1	3	A1A1	Yes	bit 0	bits 1 and 0
	2	4	A1A2	Yes	bit 1	bit 2
	3	5	A1A1	No		
	4	6	A1A2	No	none	none
	5	7	A1A1	No		
	7	1	A1A1	No		
	6	0	A1A2	No		
Upper						
Eight	10	12	A8A2	Yes	bit 3	bits 3 and 1
	11	13	A8A1	Yes	bits 3 and 0	bits 3, 1 and 0
	12	14	A8A2	No		
	13	15	A8A1	No		
	14	16	A8A2	No		
	15	17	A8A1	No		
	16	10	A8A2	No		
	17	11	A8A1	No		

Table VIII. Input/Output Signals-Mode Selection

Input/Output Mode	PROGRAM SKIP Switches Selected	CHANNEL FUNCTION Switches	
		Output Channel	Input Channel
Normal	None	SINGLE	SINGLE
External Function	0	SINGLE	SINGLE

m. Using the oscilloscope and preamplifier, measure the output data request, output data acknowledge, the output data, input data request, and input data acknowledge signal times, timing between signals, one and zero voltage levels, and transition times. The requirements for the waveforms shall be as specified in DS 4772 for the applicable interface option. The test points for the waveforms shall be as specified in table IX.

n. Select PROGRAM SKIP 4.

o. Observe that the Computer 5-stops.

p. Release SKIP 4.

q. Select PROGRAM SKIP 0 for the External Function mode.

r. Start the Computer.

s. Using the oscilloscope and preamplifier measure the timing between the external function data and the external function acknowledge, one and zero voltage levels, and transition times. The requirements for the waveforms shall be as specified in DS 4772. The test points for the waveforms shall be as specified in table IX.

t. Select PROGRAM SKIP 4.

u. Observe that the Computer 5-Stops.

v. Release SKIP 0.

w. Repeat 3.2 steps i through v for each channel combination to be input/output signal tested in accordance with table VIIa.

x. Release all skips and stops.

y. Master Clear.

Table IX. Test Points For I/O Signals

C Register Bit	Test Points
0	*gTB2 A1
1	gTB2 A2
2	gTB2 A3
3	gTB2 A4
4	gTB2 A5
5	gTB2 A6
6	gTB2 A7
7	gTB2 A8
8	gTB2 A9
9	gTB2 A10
10	gTB2 A11
11	gTB2 A12
12	gTB2 A13
13	gTB2 A14
14	gTB2 A15
15	gTB2 A16
16	gTB2 A17
17	gTB2 A18

Table IX. Test Points for I/O Signals (Cont.)

Control Lines	Test Point Signal	Test Point Return
Channels 0, 1, 10, 11		
Output Acknowledge	* gTB2 A19	
Input Acknowledge	gTB2 A27	
Output Data Request	gTB2 E25	* gTB2 E26
Input Data Request	gTB2 F25	gTB2 F26
External Interrupt Request	gTB2 G25	gTB2 G26
External Function Acknowledge	gTB2 A20	
External Function Request	gTB2 D25	gTB2 D26
Channels 2, 3, 12, 13		
Output Acknowledge	gTB2 A21	
Input Acknowledge	gTB2 A28	
Output Data Request	gTB2 E27	gTB2 E28
Input Data Request	gTB2 F27	gTB2 F28
External Interrupt Request	gTB2 G27	gTB2 G28
External Function Acknowledge	gTB2 A22	
External Function Request	gTB1 E25	gTB1 E26
Channels 4, 5, 14, 15		
Output Acknowledge	gTB2 A23	
Input Acknowledge	gTB2 A29	
Output Data Request	gTB2 E29	gTB2 E30
Input Data Request	gTB2 F29	gTB2 F30
External Interrupt Request	gTB2 G29	gTB2 G30
External Function Acknowledge	gTB2 A24	
External Function Request	gTB1 F25	gTB1 F26
Channels 6, 7, 16, 17		
Output Acknowledge	gTB2 A25	
Input Acknowledge	gTB2 A30	
Output Data Request	gTB2 E31	gTB2 E32
Input Data Request	gTB2 F31	gTB2 F32
External Interrupt Request	gTB2 G31	gTB2 G32
External Function Acknowledge	gTB2 A26	
External Function Request	gTB1 G25	gTB1 G26

* g = chassis designation as follows:

channels 0, 2, 4, 6 - g = A1A2
channels 1, 3, 5, 7 - g = A1A1
channels 10, 12, 14, 16 - g = A8A2
channels 11, 13, 15, 17 - g = A8A1

3.3 Input/output modes test. - This test verifies the functional requirements of the input/output section of the Computer by transmitting data from one channel and receiving the data on another channel in all modes of operation. The input/output modes and combinations of modes tested are as specified in table X. The following functions of the input/output section and the Computer are also tested. Input and output buffer monitors, external functions, external interrupts, intercomputer time-out interrupt, RTC overflow, RTC monitor, and external function buffer monitors.

Table X. Input/Output Modes

Input/output Mode	Switch Settings			
	PROGRAM SKIP Switch(es) Selected	RTC DISC Switch	CHANNEL FUNCTION Switches	
			Output Channel	Input Channel
Inter-Computer**	0	Release	SINGLE	SINGLE
Single, incrementing (forward)	None	Select	SINGLE	SINGLE
Single, forward, continuous data (CD)	1	Select	SINGLE	SINGLE
Single, decrementing (backward)	2	Select	SINGLE	SINGLE
Single, backward, CD	1,2	Select	SINGLE	SINGLE
Dual, forward*	3	Select	DUAL	DUAL
Dual, backward*	2,3	Select	DUAL	DUAL
ESI, forward*	4	Select	DUAL	ESI
ESI, backward*	2,4	Select	DUAL	ESI
ESA*	3,4	Select	DUAL	ESA

*Odd channels only

**When in I/C mode only, set CHANNEL INTER-COMPUTER/CHANNEL NORMAL to the I/C position for the output channel used.

Table XI. Input/Output Test Skips and Stops

Switch(es) Selected	Program Action
SKIP 0 (see note)	Intercomputer mode
SKIP 1	Continuous Data mode
SKIP 2	Decrement (backward) Buffer mode
SKIP 3	Dual Channel mode
SKIP 4	Externally Specified Index mode
SKIP 3 and SKIP 4 together	Externally Specified Address mode
STOP 0	Stop upon error (see Appendix)
STOP 1	Stop at end of test

NOTE: When SKIP key 0 is selected, no other SKIP key should be selected. When SKIP key 0 is not selected, the intercomputer communication is by-passed and the RTC DISC switch should be selected.

3.3.1 Input/output mode test setup.-

a. Load the input/output test program (SB-10163-1) specified in the Appendix. The program skips and stops of this program shall be as specified in table XI.

b. Disconnect the cables from the input/output console and connect all channel pair combinations specified in table VIIa.

3.3.2 1219 Normal modes test.-

a. Ensure that printed wiring assembly 7104010 is located at A4A1J4G.

b. If necessary, perform 3.3.1.

c. Set RUN MODE.

d. Master Clear.

e. Set the P register equal to 01000.

f. Select PROGRAM STOP 0.

g. Set bits 12 through 9 in A_L corresponding to the output channel being tested. Begin with channel 0.

h. Set bits 3 through 0 in A_L corresponding to the input channel being tested. Begin with channel 2.

i. Operate all channel function switches to SINGLE CHANNEL.

j. Set A_U bit 15.

k. Single channel forward.

1. Start the Computer.

2. Stop the Computer using STOP 1.

3. Release STOP 1.

l. Single channel backward.

1. Select PROGRAM SKIP 2.

2. Start the Computer.

3. Stop the Computer using STOP 1.

4. Release STOP 1 and SKIP 2.

m. Intercomputer mode.

1. Select PROGRAM SKIP 0.
2. Release RIC DISC switch.
3. Operate the CHANNEL INTERCOMPUTER/CHANNEL NORMAL switch for the output channel under test to I/C.
4. Start the Computer.
5. Select STOP 1.
6. Observe that the Computer 1-Stops.
7. Release STOP 1 and SKIP 0.
8. Operate the CHANNEL INTERCOMPUTER/CHANNEL NORMAL switch for the output channel under test to NORMAL.
9. Select RIC DISC.

n. Continuous data mode forward

1. Select PROGRAM SKIP 1.
2. Start the Computer.
3. Stop the Computer using STOP 1.
4. Release STOP 1.

o. Continuous data mode backward

1. Select SKIP 2.
2. Start the Computer.
3. Stop the Computer using STOP 1.
4. Release STOP 1, SKIP 1, and SKIP 2.

NOTE: If the input/output channels selected in steps g and h are odd proceed to step p, if even go to 3.3.2 u.

p. Dual channel forward.

1. Select SKIP 3.
2. Operate the channel function switches for input and output channels under test to DUAL.
3. Start the Computer.
4. Stop the Computer using STOP 1.
5. Release STOP 1.

q. Dual channel backward.

1. Select SKIP 2.
2. Start the Computer.
3. Stop the Computer using STOP 1.
4. Release STOP 1, SKIP 2 and SKIP 3.

r. ESI forward.

1. Select SKIP 4.
2. Operate the channel function switch for the input channel under test to ESI.
3. Start the Computer.
4. Stop the Computer using STOP 1.
5. Release STOP 1.

s. ESI backward.

1. Select SKIP 2.
2. Start the Computer.
3. Stop the Computer using STOP 1.
4. Release STOP 1 and SKIP 2.

t. ESA

1. Select SKIP 3.

2. Operate the channel function switch for the input channel under test to ESA.

3. Start the Computer.

4. Stop the Computer using STOP 1.

5. Release STOP 1, SKIP 3 and SKIP 4.

u. Repeat steps 3.3.2.g through t for each channel pair combination operational in the machine and specified in table VII A.

3.3.3 1218 NTDS modes test.-

a. Turn off the power.

b. Remove printed wiring assembly 7104010 from location A4A1J4G and insert it into location A4A1J5F.

c. Turn on the power.

d. If necessary, connect the Computer as specified in figure 2 and perform 3.3.1.

e. Set RUN MODE.

f. Master Clear.

g. Set the P register equal to 01000.

h. Select PROGRAM STOP 0.

i. Set bits 12 through 9 in A_I corresponding to the output channel being tested. Begin with channel 0.

j. Set bits 3 through 0 in A_I corresponding to the input channel being tested. Begin with Channel 2.

k. Operate all channel function switches to SINGLE CHANNEL.

l. Set A_u bit 16.

m. Single channel forward.

1. Start the Computer.

2. Stop the Computer using STOP 1.

3. Release STOP 1.

n. Single channel backward.

1. Select PROGRAM SKIP 2.

2. Start the Computer.

3. Stop the Computer using STOP 1.

4. Release STOP 1 and SKIP 2.

NOTE: If the input/output channels selected are odd proceed to step o, if even go to 3.3.3 s.

o. Dual channel forward.

1. Select SKIP 3.

2. Operate the channel function switches to input and output channels under test to DUAL.

3. Start the Computer.

4. Stop the Computer using STOP 1.

5. Release STOP 1.

p. Dual channel backward.

1. Select SKIP 2.

2. Start the Computer.

3. Stop the Computer using STOP 1.

4. Release STOP 1, SKIP 2 and SKIP 3.

q. ESI forward.

1. Select SKIP 4.

2. Operate the channel function switch for the input channel under test to ESI.

3. Start the Computer.

4, Stop the Computer using STOP 1.

5. Release STOP 1.

r. ESI backward.

1. Select SKIP 2.

2. Start the Computer.

3. Stop the Computer using STOP 1.

4. Release STOP 1, SKIP 2, and SKIP 4.

s. Repeat steps 3.3.3 f through r for each channel pair combination operational in the machine and specified in table VIIa.

3.3.4 1218 normal modes test.-

a. Turn off the power.

b. Remove printed wiring assembly 7104010 from location A4A1J5F, and insert it into location A4A1J5G.

c. Turn on the power.

d. If necessary, connect the computer as specified in figure 2 and perform 3.3.1.

e. Set RUN MODE.

f. Master Clear.

g. Set the P register equal to 01000.

h. Select PROGRAM STOP 0.

i. Set bits 12 through 9 in A_L corresponding to the output channel being tested. Begin with channel 0.

j. Set bits 3 through 0 in A_L corresponding to the input channel being tested.

k. Operate all channel function switches to SINGLE CHANNEL.

l. Set A_u bit 17.

m. Single channel forward.

1. Start the Computer.

2. Stop the Computer using STOP 1.

3. Release STOP 1.

n. Single channel backward.

1. Select PROGRAM SKIP 2.

2. Start the Computer.

3. Stop the Computer using STOP 1.

4. Release STOP 1 and SKIP 2.

NOTE: If the input/output channels selected are odd proceed to step o, if even go to 3.3.4 s.

o. Dual channel forward.

1. Select SKIP 3.

2. Operate the channel function switches for input and output channels under test to DUAL.

3. Start the Computer.

4. Stop the Computer using STOP 1.

5. Release STOP 1.

p. Dual channel backward.

1. Select SKIP 2.

2. Start the Computer.

3. Stop the Computer using STOP 1.

4. Release STOP 1, SKIP 2 and SKIP 3.

q. ESI forward.

1. Select SKIP 4.

2. Operate the channel function switch for the input channel under test to ESI.

3. Start the Computer.

4. Stop the Computer using STOP 1.

5. Release STOP 1.

r. ESI backward.

1. Select SKIP 2.

2. Start the Computer.

3. Stop the Computer using STOP 1.

4. Release STOP 1, SKIP 2 and SKIP 4.

s. Repeat steps 3.3.4 i through r for each channel pair combination operational in the machine and specified in table VIIa.

t. Upon completion of testing all input/output channels operational in the machine and specified in table VIIa:

1. Turn off the power.

2. Remove printed wiring assembly 7104010 from location A4A1J5G and insert it into location A4A1J4G.

3. Turn on the power.

4. Operate all channel function switches to SINGLE CHANNEL.

5. Release STOP 0.

6. Connect the Computer as specified in figure 2.

3.4 Endurance test. - The endurance test shall consist of four hours of operating time. The first-operating hour shall be the Integrated Command-Arithmetic test, followed by three operating hours which shall be the Integrated Memory test.

3.4.1 Integrated command-arithmetic test. - The integrated command-arithmetic test shall be performed as follows (operating instructions and SKIP and STOP selections for operating the command and arithmetic tests separately shall be as specified in the Appendix, along with error displays and evaluation):

a. Select RTC DISC.

b. Select EXT SYNC DISC.

c. Load the Integrated Command-Arithmetic test program (SB-10163-2) specified in the Appendix.

d. Select PROGRAM STOP 0 (release all other PROGRAM SKIPS and STOPS).

e. Set RUN MODE.

f. Master Clear.

g. Set the 1232/1532 channel number in A_L bits 6 through 3.

h. Set A_L bit 8 if the I/O console is a 1532.

i. Set A_L bit 15.

j. Set the P register equal to 01450.

k. Start the Computer.

1. Observe that the Computer operates for one hour and that the I/O console (Item 7) types the following typeout, completing one typeout approximately every 20 minutes. See the Appendix if it is desired to modify the time between typeouts.

```
COMMAND TEST
ERROR DISPLAY AU, AL
OK, END
ARITHMETIC TEST
OK END CYCLES
```

m: Stop the Computer.

3.4.2 Integrated memory test.- The integrated memory test shall be performed as follows (operating instructions and SKIP and STOP selections for operating the control memory and main memory tests separately shall be as specified in the Appendix along with error displays and evaluation):

a. Select RTC DISC.

b. Select EXT SYNC DISC.

c. Load the Integrated Memory test program SB-10163-3 specified in the Appendix.

d. Set PROGRAM STOP 0 (release all other PROGRAM SKIPS and STOPS).

e. Set RUN MODE.

f. Master Clear.

g. If the computer has the 256 word control memory, set A_L bit 0.

h. Set the 1232/1532 channel number in A_L bits 6 through 3.

i. Set A_L bit 8 if the I/O Console is a 1532.

j. Set A_L bit 15.

k. Set A_U to the main memory size index as determined by the computer configuration, as follows:

Main Memory Size	Set A_U to
8,192	000 000
16,384	000 001
24,576	000 002
32,768	000 003
40,960	000 004
49,152	000 005
57,344	000 006
65,536	000 007

l. Set the Pregister to 01450.

m. Start the Computer.

n. Observe that the Computer operates for three hours and that Item 7 types the following typeout, completing one typeout approximately every 5 minutes (depending upon memory size of computer):

CONTROL MEMORY TEST
OK END CYCLES

MEMORY TEST
END 10 CYCLES

o. Stop the Computer.

3.5 Bootstrap programs. - Verify the bootstrap program as follows:

a. If the bootstrap assembly was removed in 2.20, continue the following sequence. If the bootstrap was not removed in 2.20, skip to step e.

b. Turn off the power.

c. Replace the bootstrap assembly removed in 2.20.

d. Turn on the power.

e. Manually read out (see 5.1) the automatic recovery program (addresses 500_8 through 537_8) and verify that each of the 32_{10} words are as specified in the procurement document and the applicable dash number of 7024774.

4. INSPECTION EVALUATION

4.1 Failures.- There shall be no failures (see 5.1) during the nonprogramed inspection. Except that one failure is allowed during the endurance test, there shall be no failures during the programed inspection. Any failure shall be followed by a post-failure maintenance period. Any post-failure maintenance period exceeding two hours shall be considered a failure.

4.2 Rejection and retest.- When a failure occurs, the inspection shall be restarted at the beginning of the subtest in which the failure occurred. When more failures than specified in 4.1 occur, the equipment shall be rejected and processed in accordance with the contract or order as implemented by the cognizant Purchaser's Representative.

4.3 Errors other than failures.- Errors (see 5.1) other than failures shall not be cause for rejection. The inspection shall be restarted at the first accessible test procedure step or program entry prior to where the error occurred.

5. NOTES

5.1 Definitions.-

5.1.1 Observe.- Only the observations specified are pertinent to the test being performed; other indicators may light and extinguish but shall not be construed as relevant indications.

5.1.2 Set.- (1) A bi-stable element in a logical ONE condition; when displayed, is denoted by a lighted indicator. (2) Momentary operation of an indicator-switch and observation of a ONE condition. (3) For a register, momentary operation of indicator-switches to place the register in a specified logical condition and observation of that condition.

5.1.3 Clear. - (1) A bi-stable element in a logical ZERO condition; when displayed, is denoted by an unlighted indicator. (2) Momentary operation of a Clear switch and observation of a ZERO condition. (3) For a register, momentary operation of the register Clear switch and observation of a ZERO condition.

5.1.4 Master Clear. - Master Clear shall clear the registers and designators and place all the logic circuits in an initial condition. The Master Clear shall consist of momentarily operating the I/O CLEAR-MASTER CLEAR switch to MASTER CLEAR.

5.1.5 I/O Clear. - I/O Clear shall clear the I/O section of the Computer. The I/O Clear shall consist of momentarily operating the I/O CLEAR-MASTER CLEAR switch to I/O CLEAR.

5.1.6 Select. - Select is the act of operating a switch so as to enable the function for which the switch is labeled. For example, when the ON-LINE switch is selected, the on-line condition shall be enabled.

5.1.7 Release. - Release is the act of operating a switch to the normal position which disables the function for which the switch is labeled.

5.1.8 Light. - Light means that an indicator which was not lighted, lights and remains lighted.

5.1.9 Start the Computer. - Starting the Computer consists of momentarily operating the RESTART/START STEP switch to START STEP and observing that the PROGRAM RUN indicator lights.

5.1.10 Stop the Computer. - Stopping the Computer shall consist of momentarily operating the SEQ STEP/STOP switch to STOP and observing that the PROGRAM RUN indicator extinguishes.

5.1.11 Program stop. - Program stops are referred to herein as "X-Stops" where X is a number from 0 through 5. When a program stop occurs, the corresponding PROGRAM STOP indicator lights and the Computer operation stops.

5.1.12 Turn on power. - Turning on power consists of momentarily operating the POWER ON/OFF switch to ON and observing that the POWER indicator lights.

5.1.13 Turn off power. - Turning off power consists of momentarily operating the POWER ON/OFF switch to OFF and observing that the POWER indicator extinguishes.

5.1.14 Load. - Unless otherwise specified herein, loading a program into the Computer shall be accomplished by using the bootstrap load procedure specified in PX 3288.

5.1.15 Manually load. - To manually load a program at "consecutive" addresses, perform the following steps:

a. Set OP STEP MODE.

b. Master Clear.

c. Set W SEQ DES.

d. Set the FUNCTION CODE register equal to 44 (store A_L).

e. Select FUNCTION REPEAT.

f. Set the P register equal to the address at which the first word is to be loaded.

g. Manually clear A_L and set the word in the A_L register.

h. Momentarily operate the RESTART/START STEP switch to START STEP.

*i. Repeat steps g and h for each of the words that are to be loaded into consecutive addresses.

j. Release FUNCTION REPEAT.

k. Master Clear.

*If the next word is not to be loaded in the next consecutive address, repeat steps f through h.

5.1.16 Manually read. - To manually read the contents of "consecutive" addresses, perform the following steps:

a. Set OP STEP MODE.

b. Master Clear.

c. Set RI SEQ DES.

d. Set the FUNCTION CODE register equal to 10 (enter A_L).

e. Select FUNCTION REPEAT.

f. Set the P register equal to the address from which the first word is to be read.

g. Momentarily operate the RESTART/START STEP switch to START STEP.

h. Observe that the A_U register displays the contents of the selected address.

*i. Repeat steps g and h for each of the words to be read from consecutive addresses.

j. Release FUNCTION REPEAT.

k. Master Clear.

5.1.17 Error. - An error is any noncompliance with this specification.

5.1.18 Failure. - The occurrence of an error stop or fault indication that can be attributed to the Computer, failure to commence an operating period following a maintenance period in the endurance test, or any other indication of improper operation shall be defined as a failure; except if caused by any of the following:

a. Operator error.

b. Power interruption or failure.

c. Test equipment failure.

d. Defective indicator lamp.

e. Any other cause which is not attributed to the Computer.

6. NOTES

Not applicable.

*If the next word is not to be read from the next consecutive address, repeat steps f through h.